REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added asynchronous timing waveform to figure 3. Updated boilerplate. ksr	04-07-04	Raymond Monnin
B	Add device type 02 which is a 5 volt tolerant version. Editorial changes throughout. tcr	06-06-27	Raymond Monnin

REV																				
SHEET																				
REV	B	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Kenneth Rice

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
04- 05- 04

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 40,000 GATES WITH 18K OF INDEPENDENT SRAM, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
B	**A**	**67268**	**5962-03250**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	03250	01	Q	X	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
_____	_____	_____/				

\V

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function
01	AT40KEL040	40,000 gate field programmable gate array
02	AT40KFL040	40,000 gate field programmable gate array, 5 V tolerant

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	160	Ceramic Quad Flat Pack
Y	See figure 1	256	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{cc}) ..... -0.5 V to 5.5 V
Voltage on any input pin (V_{IN}).....
Device type 01 ..... -0.5 V dc to 5.5 V dc
Device type 02 ..... -0.5 V dc to 7.0 V dc
Voltage on any output pin (V_{OUT}) ..... -0.5 V dc to 5.5 V dc
Storage temperature ..... -65°C to 150°C
Maximum junction temperature (T_J) ..... 150°C
Power dissipation (Pd)..... 4 W
Thermal resistance junction to case (θ_{JC}):
case X..... 5°C/W
case Y..... 3°C/W

1.4 Recommended operating conditions.

Power supply voltage range .....3.0 to 3.6 V dc (±10% V_{CCI})
Case operating temperature range (T_C) .....-55 °C to +125 °C
Storage Conditions (T_{ST}) .....30 °C, 20 to 65 % RH, dust free, original packing
High level input voltage range V_{IH} .....
Device type 01 ..... 2.2 V dc to V_{CC} +0.3 V dc)
Device type 02 ..... 2.2 V dc to 5.5 V dc
Low level input voltage range V_{IL}..... -0.3 V dc to 0.8 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201 or review at http://www.jedec.org .)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing waveforms. The timing waveforms of the asynchronous and synchronous ram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall include verifying the functionality of the device. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes that may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes that may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three (3) devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3.0 V ≤ V_{CCI} ≤ 3.6 V -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH1}	I_{OH} = -4 mA,V_{CC} = 2.7 V	1,2,3	All	2.4		V
	V_{OH2}	I_{OH} = -12 mA, V_{CC} = 3.0 V			2.4		
	V_{OH3}	I_{OH} = -16 mA,V_{CC} = 3.0 V			2.4		
Low level output voltage	V_{OL1}	I_{OL} = 4 mA,V_{CC} = 2.7 V	1,2,3	All		0.4	V
	V_{OL2}	I_{OL} = 12 mA,V_{CC} = 3.0 V				0.4	
	V_{OL3}	I_{OL} = 16 mA,V_{CC} = 3.0 V				0.4	
Low level input voltage	V_{IL}	CMOS	1,2,3	All		0.3 V_{CC}	V
		TTL				0.8	
High level input voltage	V_{IH}	CMOS	1,2,3	All	0.7 V_{CC}		V
		TTL			2.0		
High level Input current	I_{IH}	V_{IN} = 3.6 V	1,2,3	All		5	µA
	I_{IHPD}	With pull down, V_{IN} = 3.3 V	1,2,3	All		300	µA
Low level Input current	I_{IL}	V_{IN} = 0 V, V_{CC} = 3.6 V	1,2,3	All	-5		µA
	I_{ILPU}	With pull up, V_{IN} = 0 V, V_{CC} = 3.6 V	1,2,3	All	-300		µA
High level Tri-state output leakage current	I_{OZH}	V_{OUT} = 3.6 V	1,2,3	All		5	µA
	I_{OZHPD}	With pull down, V_{OUT} = 3.6 V	1,2,3	All		300	µA
High level output current	I_{OZL}	V_{OUT} = 0 V, V_{CC} = 3.6 V	1,2,3	All	-5		µA
High level output current	I_{OZLPU}	With pull up, V_{OUT} = 0 V, V_{CC} = 3.6 V	1,2,3	All	-300		µA
Standby supply current	I_{CCSB}	Unprogrammed	1,2,3	All		5	mA
Input Capacitance	$C_{I/N}$ 3/	f =1 MHz, V_{IN} = 0 V, V_{CC} = 3.3 V See 4.4.1e	1,2,3	All		10	pF
Functional tests	FT 4/		7,8A,8B	All			

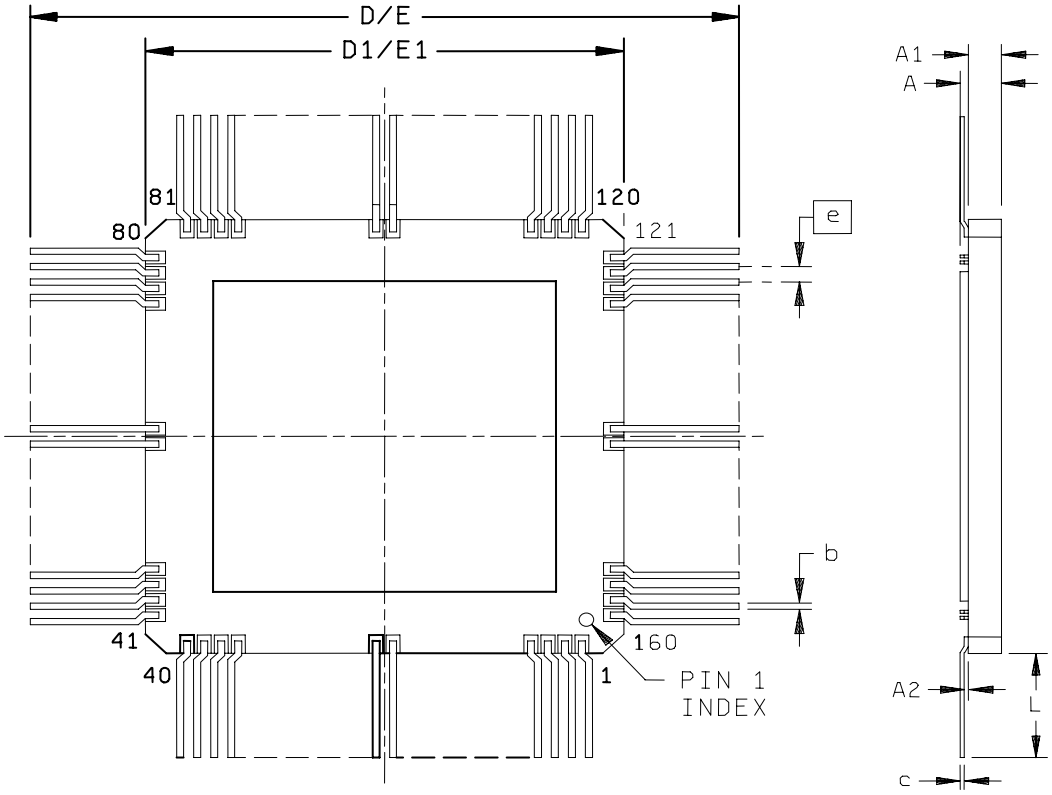
See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/ 3.0 V ≤ V_{CCI} ≤ 3.6 V -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Lut_inverter /	T_{P1}		9,10,11	All		3	ns
Lut_inverter \	T_{P2}		9,10,11	All		3	ns
Lut_buffer /	T_{P3}		9,10,11	All		3	ns
Lut_buffer \	T_{P4}		9,10,11	All		3	ns
Clock_to_q	T_{P5}		9,10,11	01		10	ns
				02		11	
Set_to_q	T_{P6}		9,10,11	01		11	ns
				02		12	
Reset_to_q	T_{P7}		9,10,11	All		13	ns

1/ Characterization data is taken at initial device introduction and repeated after any design or process changes that may affect the related parameters. Devices are first 100 percent functionally tested, and then benchmark design/timing patterns are programmed into the devices and then characterized to determine the compliance of the parameters.
2/ All tests shall be performed under the worst-case condition unless otherwise specified.
3/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore will be guaranteed to the limits set in Table 1.
4/ Devices are functionally tested using a serial scan test method.

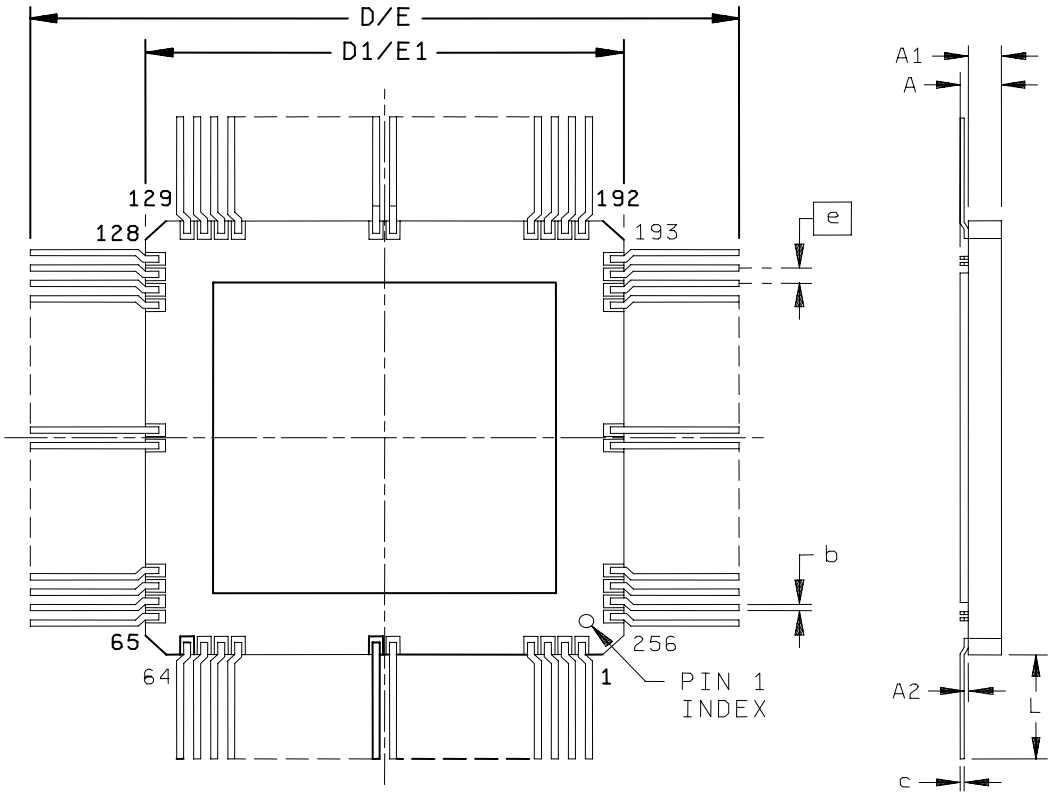
Case Outline X



	mm	
	Min	**Max**
A	1.96	2.66
A1	1.70	2.10
A2	0.10	0.30
C	0.10	0.20
D/E	37.90	39.30
D1/E1	26.90	27.50
e	0.650 BSC	
b	0.25	0.35
L	5.50	5.90
N	160	

FIGURE 1. Case outline.

Case Outline Y



	mm	
	Min	**Max**
A	2.41	3.18
A1	2.06	2.56
A2	0.05	0.36
C	0.10	0.20
D/E	53.23	55.74
D1/E1	36.83	37.34
e	0.508 BSC	
b	0.15	0.25
L	8.20	9.20
N	256	

FIGURE 1. Case outline Continued.

Case Outline X

Case outline	X		
Pin Number	Name	Pin Number	Name
1	Vcc	41	V_{CC}
2	I/O384_ GCK8_A15	42	CCLK
3	I/O383_A14	43	I/O288_GCK6
4	I/O382	44	I/O287_D0
5	I/O381	45	I/O286
6	I/O372_A13	46	I/O285
7	I/O371_A12	47	I/O278
8	I/O370	48	I/O277_D1
9	I/O369	49	I/O274
10	GND	50	I/O273
11	I/O360	51	GND
12	I/O359	52	I/O262_FCK4
13	I/O348_A11	53	I/O261
14	I/O347_A10	54	I/O260
15	I/O344	55	I/O259_D2
16	I/O343	56	I/O246
17	I/O338_A9	57	I/O245
18	I/O337_A8	58	I/O242_CHECK
19	Vcc	59	I/O241_D3
20	GND	60	GND
21	I/O336_A7	61	Vcc
22	I/O335_A6	62	I/O240
23	I/O330	63	I/O239_D4
24	I/O329	64	I/O236
25	I/O328	65	I/O235
26	I/O326_A5	66	I/O222_CS0
27	I/O325_A4	67	I/O221_D5
28	I/O314	68	I/O220
29	I/O313	69	I/O219_FCK3
30	GND	70	GND
31	I/O304	71	I/O208
32	I/O303	72	I/O207
33	I/O298_A3	73	I/O206
34	I/O297_CS1_A2	74	I/O205_D6
35	I/O292	75	I/O196
36	I/O291	76	I/O195
37	I/O290_GCK7_A1	77	I/O194_GCK5
38	I/O289_A0	78	I/O193_D7
39	GND	79	RESETN
40	TEST CLOCK	80	Vcc

FIGURE 2. Terminal connections.

Case outline		X	
Pin Number	Name	Pin Number	Name
81	CON	121	M0
82	GND	122	GND
83	I/O192_GCK4	123	M1
84	I/O191_D8	124	I/O96_GCK2
85	I/O190	125	I/O95_OTS
86	I/O189	126	I/O94
87	I/O184_D9	127	I/O93
88	I/O183_D10	128	I/O90
89	I/O180	129	I/O89
90	I/O179	130	I/O84
91	GND	131	I/O83
92	I/O168	132	GND
93	I/O167	133	I/O72_FCK2
94	I/O166_D11	134	I/O71
95	I/O165_D12	135	I/O70
96	I/O152	136	I/O69
97	I/O151	137	I/O54
98	I/O146_D13	138	I/O53
99	I/O145_D14	139	I/O50
100	GND	140	I/O49
101	Vcc	141	Vcc
102	I/O144_INIT	142	GND
103	I/O143_D15	143	I/O48_A23
104	I/O138	144	I/O47_A22
105	I/O137	145	I/O44
106	I/O124	146	I/O43
107	I/O123	147	I/O28_A21
108	I/O122	148	I/O27_A20
109	I/O121	149	I/O26
110	GND	150	I/O25_FCK1
111	I/O110	151	GND
112	I/O109	152	I/O16
113	I/O102_LDC	153	I/O15
114	I/O101	154	I/O6_A19
115	I/O100	155	I/O5_A18
116	I/O99	156	I/O4
117	I/O98_HDC	157	I/O3
118	I/O97_GCK3	158	I/O2_A17
119	M2	159	I/O1_GCLK1_A16
120	Vcc	160	GND

FIGURE 2. Terminal connections – Continued.

Case Outline Y

Case outline	Y		
Pin Number	Name	Pin Number	Name
1	I/O384_ GCK8_A15	41	I/O324
2	I/O383_A14	42	I/O323
3	I/O382	43	I/O321
4	I/O381	44	I/O320
5	I/O378	45	I/O318
6	I/O377	46	I/O317
7	GND	47	I/O314
8	Vcc	48	I/O313
9	I/O375	49	I/O312
10	I/O374	50	I/O311
11	I/O372_A13	51	I/O308
12	I/O371_A12	52	I/O307
13	I/O370	53	I/O304
14	I/O369	54	I/O303
15	I/O366	55	I/O301
16	I/O365	56	I/O298_A3
17	I/O362	57	GND
18	I/O360	58	Vcc
19	I/O359	59	I/O297_CS1_A2
20	I/O358	60	I/O291
21	I/O356	61	I/O292
22	I/O355	62	I/O290_GCK7_A1
23	I/O353	63	I/O289_A0
24	I/O352	64	TESTCLOCK
25	I/O349	65	CCLK
26	I/O348_A11	66	I/O288_GCK6
27	I/O347_A10	67	I/O287_D0
28	I/O346	68	I/O286
29	I/O344	69	I/O285
30	I/O343	70	I/O282
31	I/O338_A9	71	GND
32	I/O337_A8	72	Vcc
33	I/O336_A7	73	I/O278
34	I/O335_A6	74	I/O277_D1
35	I/O334	75	I/O276
36	I/O330	76	I/O274
37	I/O329	77	I/O273
38	I/O328	78	I/O272
39	I/O326_A5	79	I/O270
40	I/O325_A4	80	I/O269

FIGURE 2. Terminal connections – Continued.

Case outline		Y	
Pin Number	Name	Pin Number	Name
81	I/O267	121	GND
82	I/O266	122	Vcc
83	I/O26_FCK4	123	I/O203
84	I/O261	124	I/O196
85	I/O260	125	I/O195
86	I/O259_D2	126	I/O194_GCK5
87	I/O258	127	I/O193_D7
88	I/O257	128	RESETN
89	I/O254	129	CON
90	I/O253	130	I/O192_GCK4
91	I/O252	131	I/O191_D8
92	I/O251	132	I/O190
93	I/O248	133	I/O189
94	I/O246	134	I/O186
95	I/O245	135	GND
96	I/O242_CHECK	136	Vcc
97	I/O241_D3	137	I/O184_D9
98	I/O240	138	I/O183_D10
99	I/O239_D4	139	I/O181
100	I/O236	140	I/O180
101	I/O235	141	I/O179
102	I/O234	142	I/O177
103	I/O232	143	I/O174
104	I/O230	144	I/O173
105	I/O228	145	I/O171
106	I/O227	146	I/O168
107	I/O225	147	I/O167
108	I/O224	148	I/O166_D11
109	I/O222_CS0	149	I/O165_D12
110	I/O221_D5	150	I/O163
111	I/O220	151	I/O162
112	I/O219_FCK3	152	I/O161
113	I/O216	153	I/O158
114	I/O215	154	I/O157
115	I/O212	155	I/O156
116	I/O208	156	I/O152
117	I/O207	157	I/O151
118	I/O206	158	I/O150
119	I/O205_D6	159	I/O149
120	I/O204	160	I/O146_D13

FIGURE 2. Terminal connections – Continued.

Case outline	Y		
Pin Number	Name	Pin Number	Name
161	I/O145_ D14	201	I/O90
162	I/O144_INIT	202	I/O89
163	I/O143_D15	203	I/O86
164	I/O141	204	I/O85
165	I/O138	205	I/O84
166	I/O137	206	I/O83
167	I/O136	207	I/O80
168	I/O134	208	I/O79
169	I/O132	209	I/O77
170	I/O131	210	I/O76
171	I/O129	211	I/O72_FCK2
172	I/O128	212	I/O90
173	I/O124	213	I/O71
174	I/O123	214	I/O70
175	I/O122	215	I/O69
176	I/O121	216	I/O67
177	I/O120	217	I/O66
178	I/O119	218	I/O63
179	I/O116	219	I/O62
180	I/O115	220	I/O60
181	I/O113	221	I/O59
182	I/O110	222	I/O57
183	I/O109	223	I/O56
184	I/O101	224	I/O54
185	GND	225	I/O53
186	Vcc	226	I/O50
187	I/O102_LDC	227	I/O49
188	I/O99	228	I/O48_A23
189	I/O100	229	I/O47_A22
190	I/O98_HDC	230	I/O44
191	I/O97_GCK3	231	I/O43
192	M2	232	I/O41
193	M0	233	I/O39
194	M1	234	I/O36
195	I/O96_GCK2	235	I/O35
196	I/O95_OTS	236	I/O34
197	I/O94	237	I/O33
198	I/O93	238	I/O30
199	GND	239	I/O28_A21
200	Vcc	240	I/O27_A20

FIGURE 2. Terminal connections – Continued.

Case Outline Y - Continued.

Case outline		Y	
Pin Number	Name	Pin Number	Name
241	I/O26	249	GND
242	I/O25_FCK1	250	Vcc
243	I/O21	251	I/O6_A19
244	I/O20	252	I/O5_A18
245	I/O18	253	I/O4
246	I/O16	254	I/O3
247	I/O15	255	I/O2_A17
248	I/O13	256	I/O1_GCLK1_A16

FIGURE 2. Terminal connections – Continued.

Synchronous timing characteristics

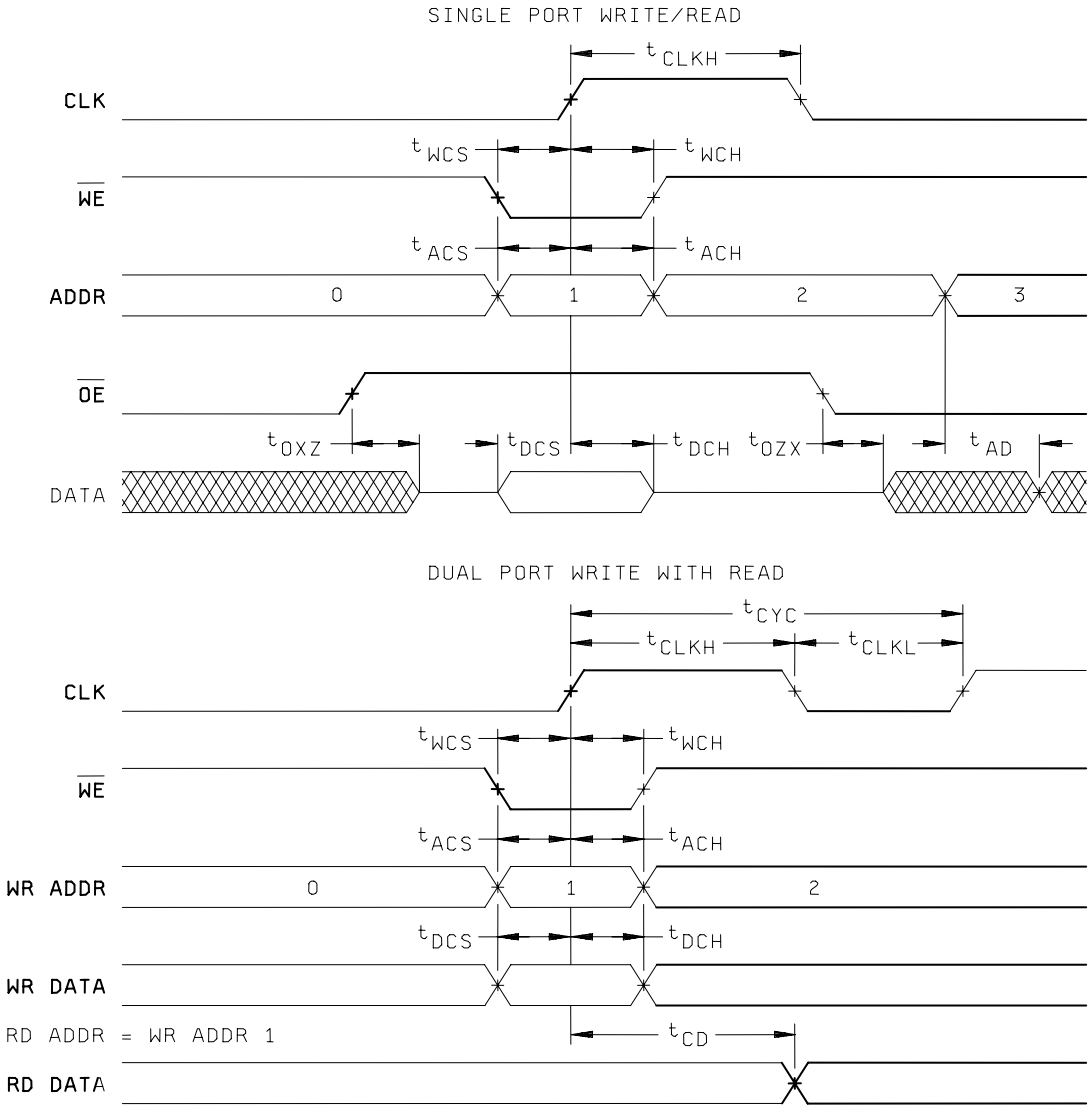


FIGURE 3. Timing waveforms.

Asynchronous timing characteristics

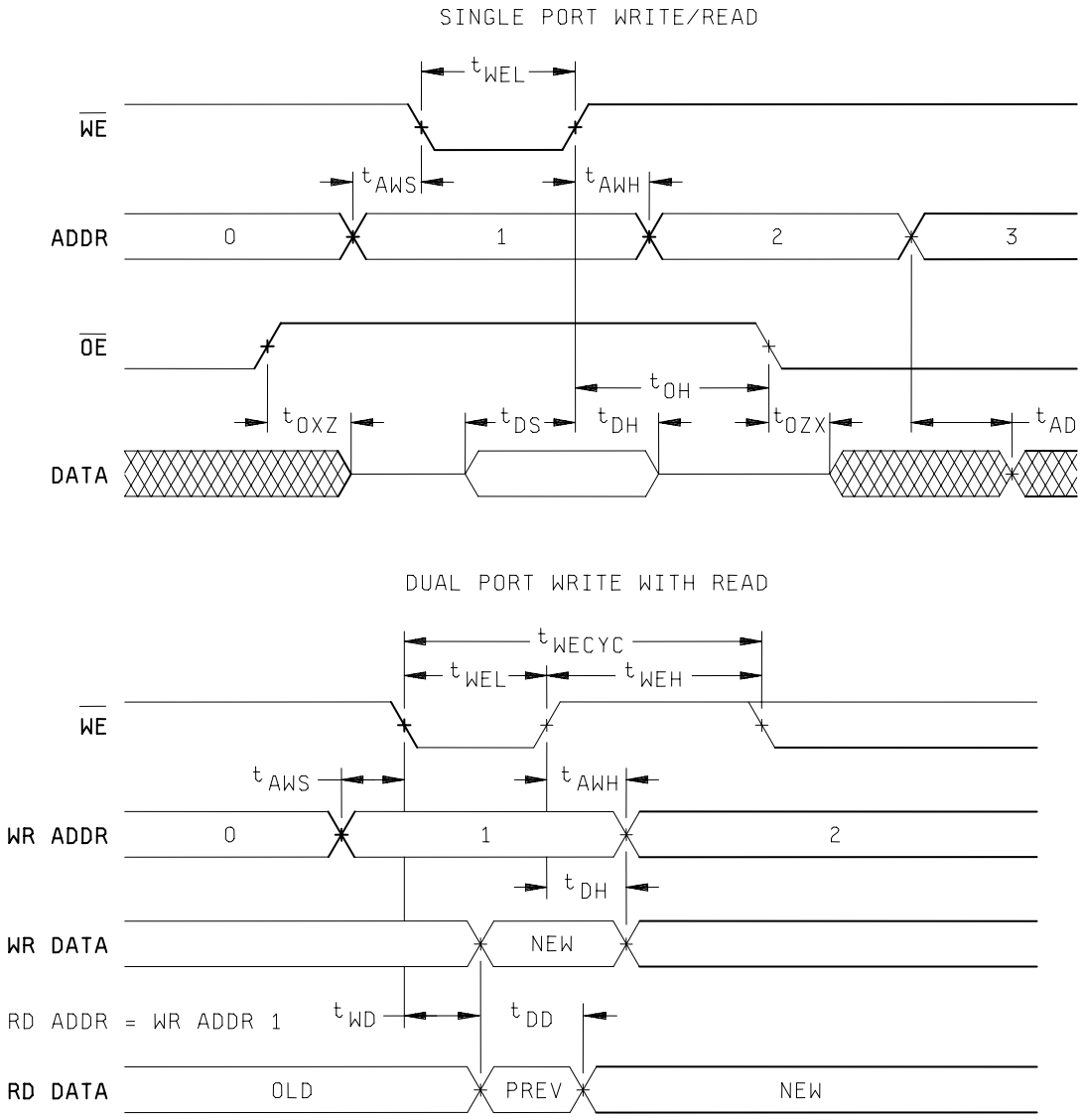


FIGURE 3. Timing waveforms - Continued.

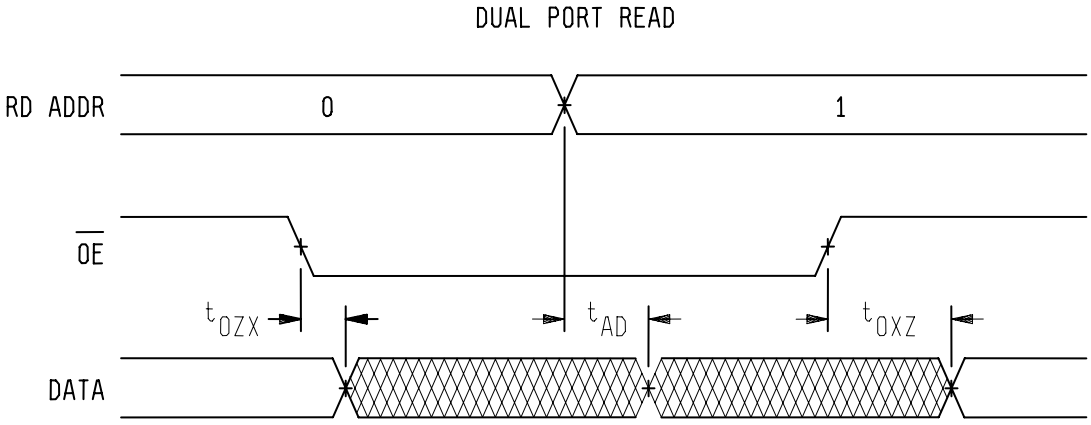


FIGURE 3. Timing waveforms - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1e.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCSB}	± 0.5 mA of specified value in table I
I_{IL}/I_{IH}	± 0.5uA of specified value in table I
V_{OL}/V_{OH}	± 0.1 V of specified value in table I
I_{OZ}	± 0.5uA of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-27

Approved sources of supply for SMD 5962-03250 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0325001QXC	F7400	AT40KEL040KW1MQ
5962-0325001VXC	F7400	AT40KEL040KW1SV
5962-0325001QYC	F7400	AT40KEL040KZ1MQ
5962-0325001VYC	F7400	AT40KEL040KZ1SV
5962-0325002QXC	F7400	AT40KFL040KW1MQ
5962-0325002VXC	F7400	AT40KFL040KW1SV
5962-0325002QYC	F7400	AT40KFL040KZ1MQ
5962-0325002VYC	F7400	AT40KFL040KZ1SV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes BP 70602 Route De Gachet 44306 Nantes Cedex 03 Nantes, France 44100